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P(VDF/TrFE) copolymer films for the fabrication of pyroelectric arrays

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Abstract

Linear pyroelectric arrays with poly(vinylidene fluoride/trifluorethylene), P(VDF/TrFE), copolymer films on integrated CMOS circuits are described. The maximum specific detectivity of the sensors is of the order of 10^7 cm $\sqrt{\text{Hz}}$/W. A new technology for the deposition and the patterning of the copolymer layers on the readout chip is described. This device technology allows the copolymer layers to be poled on the chip.

1. Introduction

Pyroelectric sensor arrays on silicon integrated circuits have been investigated and advanced during recent years [1]. In an earlier paper a linear 8 × 1 array based on a poly(vinylidene fluoride), PVDF, layer and a p-well CMOS process with aluminium gates was described [2]. In this case, a pyroelectric PVDF foil was glued to the chip.

An improvement of the technology of integrated pyroelectric sensor arrays is achieved by coating the silicon wafers with pyroelectric poly(vinylidene fluoride/trifluorethylene) P(VDF/TrFE), films. The copolymer films may also serve as (passive) interlayers in order to reduce the thermal and capacitive coupling. In this contribution, the deposition and the patterning processes of P(VDF/TrFE) layers with the compositions 50/50, 65/35 and 75/25 are described. The thickness of these copolymer films is in the 1–10 μm range. The success of the wet etching process is strongly dependent on the composition, the concentration and the temperature of the etching solution.

A pyroelectric sensor element consists of a pyroelectric layer with aluminium electrodes on both surfaces. The bottom electrode is connected to the readout circuit integrated into the silicon substrate. This requires the patterning of a stack of different materials. As a technological realization, a combination of wet and dry etching processes is discussed. This device technology allows the on-chip poling of the copolymer layers to be achieved. In the present investigation, the conventional method of poling at room temperature was performed with evaporated metal electrodes [3]. The highest pyroelectric activities were obtained by poling at the highest fields. The maximum field, however, is limited by local breakdown. The technological requirements to achieve high pyroelectric activity are discussed. Finally, results of measurements of the pyroelectric properties are presented.

2. Technology

The starting material of the CMOS process is n-type silicon. The p-well is formed by a two-step boron implantation followed by a drive-in step. The source and drain regions of the NMOS and PMOS transistors are obtained by two-step diffusions. Gate resistors with a value of the order of 10^{10} Ω are required in order to adjust the operating point of the MOSFETs. These devices are realized by p–n junctions operated at zero bias. The characteristics are tailored by deliberate radiation damage, i.e., helium implantation followed by annealing in a nitrogen atmosphere. A detailed description of the CMOS process is given in ref. 2. A simplified cross section of a complete sensor element is shown in Fig. 1.

Previously, a 25 μm thick PVDF foil was used as the pyroelectric material, which was glued to the contact metallization of the chip after dicing of the wafers. In order to reduce the costs in the sensor fabrication and for an integration of the sensor element and the readout circuit, it is necessary to utilize the well-known production steps for integrated circuits also for the preparation of the sensor elements. This is possible by introducing P(VDF/TrFE) copolymer films as the pyroelectric material. These layers can be applied to silicon wafers by spin

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